PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

M

To:
AJAY JAGTIANI
10363-A DEMOCRACY LANE
FAIRFAX, VA 22030

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing (*day/month/year*) 06 APR 2005
Applicant's or agent's file reference KAGU-0002-2	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US04/15877	International filing date (*day/month/year*) 20 May 2004 (20.05.2004)
Applicant KAGUTECH LTD.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 740 14 35

   For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/ US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Prabodh Dharia Telephone No. 571-272-7668

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference KAGU-0002-2	**FOR FURTHER ACTION** see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/US04/15877	International filing date (*day/month/year*) 20 May 2004 (20.05.2004)	(Earliest) Priority Date (*day/month/year*) 20 May 2003 (20.05.2003)
Applicant KAGUTECH LTD.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 9 sheets.

☒ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the Report**
   a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.
      ☐ The international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).
   b. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (See Box No. II)
3. ☒ **Unity of invention is lacking** (See Box No. III)
4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☐ the text is approved as submitted by the applicant.
   ☒ the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,
   a. the figure of the drawings to be published with the abstract is Figure No. 16
      ☐ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☒ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

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Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
Please See Continuation Sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest
☐ The additional search fees were accompanied by the applicant's protest.
☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US04/15877

Box IV TEXT OF THE ABSTRACT (Continuation of Item 5 of the first sheet)

The present invention provides a digital backplane and various methods, systems and devices for controlling a digital backplane and light modulating elements (figure 16). In somes embodiments of the present invention, a recursive feedback method is used to control a digital backplane and/or spatial light modulator.

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A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : G09G 03/36
US CL : 345/87,467,100,542, 364/413,372/92,359/141,166,382/54,399/74,49,348/614,455/52.3,340/635
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 345/87,467,100,542, 364/413,372/92,359/141,166,382/54,399/74,49,348/614,455/52.3,340/635

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,585,816 (Schaffer et al.) 17 December 1996 (17.12.1996)Col. 3, Lines 43-67, Col. 5, Line 42 to Col. 6, Line 67, Col. 10, Line 1 to col. 11, Line 43	1-15, 30-159
Y	6,542,142 B2 (Yumoto et al.) 1 April 2003 (01.04.2003) Col. 3, Line 39 to Col. 4, Line 9, Col. 5, Line 19-32, Col. 10, Line 61 to Col. 12, Line 9, Col. 12, Lines 49-63,Col. 13, Line 55 to Col. 15, Line 2, Col. 17, Line 53 to Col. 18, Line 51, Col. 18, Line 66 to col. 19, Line 9, Col. 25, line 31-37, Col. 26, Line 54 to Col. 27, Line 3, Col. 34, Lines 20-60, Col. 39, Lines 4-48, Col. 41, Lines 37-50	1-30
Y	US 4,847,854 (Van Dijk) 11 July 1989 (11.07.1989) Col. 4, Lines 4-6, Col. 14, lines 51-56, Col. 15, Lines 13-68, Col. 16, lines 17-60, Col. 2, lines 10-15, Col. 17, Lines 10-41, Col. 28, Lines 8-13, Col. 5, Lines 4-18, Col. 27, Lines 20-25	1-15,90-100
Y	US 20022039800 (Kang S. G.) 30 May 2002 (30.05.2002) page 2 detailed description.	15, 30-38, 47-84
Y	US 4,364,093 (Holmes) 14 December 1982 (14.12.1982) Col. 3, Lines 29 -67, Col. 4, Line 26 to Col. 5, Line 54	16-38,152-168
Y	US 5,920,322 (Ulichney) 6 July 1999 (6.07.1999), Col. 6, Lines 15-67, Col. 8, line 39 to Col. 12, Line 28	16-84

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
07 March 2005 (07.03.2005)	06 APR 2005
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Prabodh Dharia Telephone No. 571-272-7668

Form PCT/ISA/210 (second sheet) (January 2004)

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International application No.
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C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,581,272 (Conner et al.) 03 December 1996 (03. 12.1996) Col. 3, Line 3 to Col. 6, Line 33, Col. 8, Lines 11-37	46-88
Y	US 4,742,552 (Andrews) 05 May 1988 (05.05.1988) Col. 29, Line 27 to Col. 36, Line 10, Col. 27, Line 3 to Col. 29, Line 25	65-100
Y	US 6,107,979 (Chiu et al.) 22 August 2000 (22.08.2000) Col. 6, Line 29 to Col. 8, Line 67, Col. 10, Lines 14-58, Col. 11, Line 31 to Col. 15, Line 13	89,126-130,142-151
Y	US 6,118,500 (Kunzman) 12 September 2000 (12.09.2000) Col. 4, Line 55 to Col. 7, Line 54, Col. 8, Line 21 to Col. 10, Line 2	101-119
Y	US 6,023,263 (Wood) 08 February 2000 (08.02.2000) Col. 5, Line 3 to Col. 8, Line 9	101-119,142-151,160-168
Y	US 20010043177 A1 (Huston et al.) 22 November 2001 (22.11.2001) page 3, paragraphs 24-31, 33-34, Pge 4, paragraphs 34-40, page 5, paragraphs 81 to page 7, paragrph 102, page 8, paragraph 113 to page 10, paragarph 137, page 10, paragraph 141 to page 12, paragraph 161, page 17, paragraphs 257-263, page 18, paragraph263 to page 19, paragraph 285	101-151
Y	US 5,576,873 (Crossland et al.) 19 November 1996 (19.11.1996) Col. 4, Line 17 to Col. 6, Line 42, Col. 8, Line35 to Col. 10, Line 2, Col. 15, Lines 3 to Col. 16, Line 10	120-125
Y	US 6,046,719 (Dingwall) 04 April 2000 (04.04.2000) Col. 5, Line 18 to Col./ 6, Line 15, Col. 11, Line 49 to Col. 12, Line 11, Col. 12, Line 40 to Col. Col. 14, Line 27	126-130
Y	US 6,061,049 (Pettitt et al.) 09 May 2000 (09.05.2000) Col. 2, Lines 1-14, Col. 1, Linesa 46-60, Col. 6, Line 19 to Col. 7, Line 50	126-130
Y	US 6,762,873 B1 (Coker et al.) 29 June 2000 (29.06.2000) Col. 3, Line 64 to Col. 5, Line 26, Col. 11, Line 14 to Col. 13, Line 55, Col. 23, Line 29 to Col. 24, Line 8	131-151
Y	US 5,771,060 (Nelson) 23 June 1998 (23.06.1998) Col. 6, Line 31 to Col. 8, Line 25	152-168
Y	US 6,717,222 (Zhang) 10 April 2003 (10.04.2003) Col. 10, Line 65 to Col. 11, Line 51	160-168
Y	US 6,329,987 B1 (Gotfried et al.) 11 December 2001 (11.12.2001) Col. 12, Line 34 to col. 13, Line 12, Col. 14, Lines 49-67	160-168
Y	US 6,809,734 B2 (Suzuoki et al.) 26 September 2002 (26.09.2002) Col. 15, Line 34 to Col. 18, Line 24	160-168

INTERNATIONAL SEARCH REPORT

International application No.
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BOX III. OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING

This appilcation contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

I. Claims 1-15 are drawn to display driving by controlling light modulating element.
II. Claims 16-29,142,143 are drawn to display, with series of stages each having stage value corresponding to pixel value of light modulating element.
III Claims 30-38 are drawn to display with storage bits corresponding to pixel value of light modulating element and mask write operation as updating means which also performs setting and resetting.
IV Claims 39-47 are drawn to display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element.
V Claims 48-67 are drawn to display with logical bit serial operation such as arithmetic.
VI Claims 68-89 are drawn to two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value.
VII Claims 90-125 are drawn to method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator.
VIII Claims 126-130 are drawn to digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element.
IX Claims 131-141 are drawn to array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements.
X Claims 144-157 are drawn to a spatial light modulator comprising an array of master slave bit pair stored in MRAM.
XI Claims 158-160 are drawn to Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.
XII Claims 161-168 are drawn to MRAM array storage bits arranged in MRAM columns.

The inventions are distinct, from each other listed in Groups I-XII and do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2 they lack the same or corresponding special technical features for the following reasons:

Invention I relates a display unit driving by controlling light modulating element; however, it does not relate to display with logical bit serial operation such as arithmetic, spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference or series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM.

Invention II relates relate series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator; however, it does not relate to display with logical bit serial operation such as arithmetic, reallocating available memory for

data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention III relates to display with storage bits corresponding to pixel value of light modulating element and mask write operation as updating means which also performs setting however, it does not relate to stage value corresponding to pixel value or providing memory on a spatial light modulator; reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention IV relates to display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element, however, it does not relate to display unit driving by controlling light modulating element; stage value corresponding to pixel value or providing memory on a spatial light modulator; reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention V relates to display with logical bit serial operation such as arithmetic, however, it does not relate to display unit driving by controlling light modulating element; stage value corresponding to pixel value or providing memory on a spatial light modulator; reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference.

Invention VI relates to two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value, however, it does not relate to display with logical bit serial operation such as arithmetic, spatial light modulator comprising an array of master slave bit pair stored in MRAM or Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference or series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator or spatial light modulator comprising an array of master slave bit pair stored in MRAM.

Invention VII relates to method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, however, it does not relate to digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements.

Invention VIII relates to digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, however, it does not relate to method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, a spatial light modulator comprising an array of master slave bit pair stored in MRAM, or two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value.

Invention IX relates to array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, however, it does not relate to Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, a spatial light modulator comprising an array of master slave bit pair stored in MRAM, or MRAM array storage bits arranged in MRAM columns.

Invention X relates to a spatial light modulator comprising an array of master slave bit pair stored in MRAM, however, it does not relate to display with logical bit serial operation such as arithmetic, digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator or display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element.

Invention XI relates to Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, however, it does not relate to display with logical bit serial operation such as arithmetic, digital back plane storing first and second groups of bit position corresponding to pixel values and combining to control pulse width of light modulating element, method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator, display with two series of count steps LS count steps and MS count steps setting or clearing output bits to set pixel values for array of light modulating element or MRAM array storage bits arranged in MRAM columns; series of stages each having stage value corresponding to pixel value or providing memory on a spatial light modulator.

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Invention XII relates to MRAM array storage bits arranged in MRAM columns, however, it does not relate to a display unit driving by controlling light modulating element; Mapping of first and second pixel values with time base to generate pulse width to reduce phase difference, a spatial light modulator comprising an array of master slave bit pair stored in MRAM, array of circuits comprising means for voltage level shifting with a selectable logic function based on memory bit; and means for controlling light modulating elements, method comprising of providing memory on a spatial light modulator; and reallocating available memory for data on spatial light modulator; two dimensional light array of light modulating element with means for computing a one dimensional array of control signals for output bits based on one or more sets one bit positions of pixel value.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
AJAY JAGTIANI
10363-A DEMOCRACY LANE
FAIRFAX, VA 22030

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing (*day/month/year*)	06 APR 2005
Applicant's or agent's file reference KAGU-0002-2	FOR FURTHER ACTION See paragraph 2 below

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/US04/15877	20 May 2004 (20.05.2004)	20 May 2003 (20.05.2003)

International Patent Classification (IPC) or both national classification and IPC

IPC(7): G09G03/36 and US Cl.: 345/87,100

Applicant

KAGUTECH LTD.

1. This opinion contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☒	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☒	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(*b*) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/ US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Prabodh Dharia Telephone No. 571-272-7668

Form PCT/ISA/237 (cover sheet) (January 2004)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US04/15877

Box No. I Basis of this opinion

1. With regard to the language, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

☐ This opinion has been established on the basis of a translation from the original language into the following language _____, which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

a. type of material

☐ a sequence listing

☐ table(s) related to the sequence listing

b. format of material

☐ in written format

☐ in computer readable form

c. time of filing/furnishing

☐ contained in international application as filed.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

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Box No. IV Lack of unity of invention

1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees the applicant has:
   - ☒ paid additional fees
   - ☐ paid additional fees under protest
   - ☐ not paid additional fees
2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.
3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is
   - ☒ complied with
   - ☐ not complied with for the following reasons:

   Applicant has paid additional fees in timely manner.

4. Consequently, this opinion has been established in respect of the following parts of the international application:
   - ☒ all parts.
   - ☐ the parts relating to claims Nos. _____

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US04/15877

Box No. V Reasoned statement under Rule 43 *bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims NONE	YES
	Claims 1-168	NO
Inventive step (IS)	Claims NONE	YES
	Claims 1-168	NO
Industrial applicability (IA)	Claims 1-168	YES
	Claims NONE	NO

2. Citations and explanations:

Please See Continuation Sheet

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US04/15877

Box No. VI Certain documents cited

1. Certain published documents (Rules 43*bis*.1 and 70.10)

Application No. Patent No.	Publication date (day/month/year)	Filing date (day/month/year)	Priority date (valid claim) (day/month/year)
6,809,734 B2	26-09-2002	22-03-2001	
6,329,987 B1	11-12-2001	02-12-1998	
6,717,222, B2	10-04-2003	28-08-2002	08-04-2002
5,771,060	23-06-1998	07-06-1995	19-12-1998
6,762,873 B1	29-06-2000	16-12-1999	
6,061,049	09-05-2000	07-07-1999	
6,046,719	04-04-2000	20-08-1998	
5,576,873	19-11-1996	27-07-1993	01-08-1992
20010043177 A1	22-11-2001	14-12-2000	
6,023,263	08-02-2000	05-06-1997	07-06-1996
6,118,500	12-09-2000	28-08-1997	
6,107,979	22-06-2000	03-04-1997	
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2. Non-written disclosures (Rules 43*bis*.1 and 70.9)

Kind of non-written disclosure	Date of non-written disclosure (day/month/year)	Date of written disclosure referring to non-written disclosure (day/month/year)

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V. 2. Citations and Explanations:
Claims 1-15 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Scheffer et al. in view of Yumamoto et al. VanDijk and Kang et al.

Schefer et al. teaches; display driver driving electrode using a pulse width controlled by recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel data based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends. Yumamoto et al. teaches; display diver driving electrode using a pulse width to thereby comntrolling a pixel of a spatial light modulating element according to pixel data based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and teaches display having semiconductor substrate. VanDijk teaches panel interface controller with recursive feedback, of a visual display that includes array of light emitting elements on a single silicon backplane. Kang et al. teaches LCOS LCD apparatus where liquid crystal material includes includes PH to indicate damage to visual display. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 16-301acks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Holmes in view of Yumoto et al. and Ulichney.

Holmes teaches a display unit driving by controlling light modulating element, display interface controller with recursive feedback of a visual display that includes array of lght modulating elements. Yumamoto et al. teaches display driver driving electrode using a pulse width to thereby controlling a pixel of a spatial light modulating element according to pixel data based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive a pixel electrode and teaches display having semiconductor substarte. Ulichney teaches series of stages with ech stage having value associated with subsets of bits of pixels value of light modulating element. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 30-38 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Holmes in view of Scheffer et al., Ulicinmey and Kang et al.

Holmes teaches a display unit driving by controlling light modulating element, display interface controller with explicit recursive feedback of a visual display that includes array of lght modulating elemens. Schefer et al. teaches; display driver driving electrode using a pulse width controlled by implicit recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel data based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and teaches display having semiconductor substrate. Ulichney teaches series of stages with each stage having value associated with subsets of bits of pixels value fo light modulating element. Kang et al. teaches LCOS LCD apparatus where liquid crystal material

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includes includes PH to indicate damage to visual display. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 39-46 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Scheffer et al. in view of Ulichne .

Schefer et al. teaches; display driver driving electrode using a pulse width controlled by recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel data based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends. Ulichney teaches series of stages with each stage having value associated with subsets of bits of pixels value to light modulating element. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 47-64 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Scheffer et al. in view of Ulichney, Conner et al., Andrews and Kang et al.

Schefer et al. teaches; display driver driving electrode using a pulse width controlled by recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel data based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends. Ulichney teaches series of stages with each stage having value associated with subsets of bits of pixels value of light modulating element. Conner et al. teahes grouping of the array, reseting the light modulating elements, and pulse width modulation controling signal through electrodes to control light modulating element. Andrews teaches two dimensional array as well as one dimensional array, and bit serially processing. Kang al. teaches LCOS LCD apparatus where liquid crystal material include includes PH to indicate damage to visual display. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 65-75 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Scheffer et al. in view of Ulichney, Conner et al., Andrews and Kang et al.

Schefer et al. teaches; display driver driving electrode using a pulse width controlled by recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel data based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements. Ulichney teaches series of stages with ech stage having value associated with subsets of bits of pixels value of light modulating element. Conner et al. teahes grouping of the array, reseting the light modulating elements, and pulse width modulation controling signal through electrodes to control light modulating element. Andrews teaches two dimensional array as well as one dimensional array, and bit serially processing. Kang et al. teaches LCOS LCD apparatus where liquid crystal material includes includes PH to indicate damage to visual display. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 76-84 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Scheffer et al. in view of Ulichney, Conner et al., Andrews and Kang et al.

Schefer et al. teaches; display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements. Ulichncy teaches series of stages with each stage having value associated with subsets of bits of pixels value of light modulating element and performed series of stages controlled by computer command or instructions. Conner et al. teahes grouping of the array, reseting the light modulating elements, and pulse width modulation controling signal through electrodes to control light modulating element. Andrews teaches two dimensional array as well as one dimensional array, bit serially processing and fully digitally encoded pixel values and controlling multiple data path. Kang et al. teaches LCOS LCD apparatus where liquid crystal material includes includes PH to indicate damage to visual display. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 85 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Scheffer et al. in view of Conner et al. and Andrews .

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Schefer et al. teaches; display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements. Conner et al. teahes grouping of the array, reseting the light modulating elements, and pulse width modulation controling signal through electrodes to control light modulating element. Andrews teaches two dimensional array as well as one dimensional array, bit serially processing and fully or partially digitally encoded pixel values and controlling multiple data path. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 86-88 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Scheffer et al, in view of Conner et al. and Andrews .

Schefer et al. teaches; display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and ulse width ends also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements. Conner et al. teahes grouping of the array, reseting the light modulating elements, and pulse width modulation controling signal through electrodes to control light modulating element. Andrews teaches two dimensional array as well as one dimensional array, bit serially processing and fully or partially digitally encoded pixel values and controlling multiple data path. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 89 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Scheffer et al. in view of Andrews .

Schefer et al. teaches; display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby comntrolling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located or the driver IC substrate which controls light modulating elements. Andrews teaches two dimensional array as well as one dimensional array, bit serially processing and fully or partially digitally encoded pixel values and controlling multiple data path. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 90-1001acks novelty under PCT article 33(2), and lacks an invcntivc stcp under PCT article 33(3) as being obvious over the combination of Scheffer et al. in view of Andrews, Chiu et al. and VanDijk.

Schefer et al. teaches; display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located or the driver IC substrate which controls light modulating elements; also teaches circular and non-circular buffer (shift register). Andrews teaches two dimensional array as well as one dimensional array, bit serially processing and fully or partially digitally encoded pixel values and controlling multiple data path; providing available memory pixel values. Chiu et al. teaches spatial light modulator providing memory where space is based on the length of time data needs to stay resident. VanDijk teaches panel interface controller with recursive feedback, of a visual display that includes array of light emitting elements on a single silicon backplane. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 101-119 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Hustan et al. in view of Schefer et al., Krnzma„ and Wood.

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Hustan et al. teaches; display system providing available memory on a spatial light modulator; and means for reallocating said available memory for data on said spatial light modulator, wherein space allocated is based on the length of time that said data needs to stay resident on said spatial light modulator and wherein said data is processed to control electrodes on said spatial light modulator and backplane further comprises a pointer memory array, said memory pointers are held in said pointer memory array and instruction memory, ROM and RAM. Schefer et al., display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements; also teaches circuilar and non-circular buffer (shift register). Kunzman teaches a backplane comprising an instruction memory for holding instructions for controlling at least one pulse width on each light modulating element of a spatial light modulator. Chiu teaches spatial light modulator providing memory where space is based on the length of time data needs to stay resident. Wood teaches MRAM memory array and the ROM and MRAM provide program memory and workspace for the CPU, and special processing hardware may be provided to assist the CPU to perform the large number of arithmetic operations required to convert all but the simplest models into a two dimensional scene. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 120-125 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Hustan et al. in view of Schefer et al., Crossland et al.

Hustan et al. teaches; display system providing available memory on a spatial light modulator; and means for reallocating said available memory for data on said spatial light modulator, wherein space allocated is based on the length of time that said data needs to stay resident on said spatial light modulator and wherein said data is processed to control electrodes on said spatial light modulatorand backplane further comprises a pointer memory array, said memory pointers are held in said pointer memory array; instruction memory, ROM, RAM and a backplane for a spatial modulator; a plurality of pointers to bit position array on said backplane; and pointer controller means for controlling said plurality of pointers. Schefer et al., display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements; also teaches circuilar and non-circular buffer (shift register). Crossland et al. teaches a backplane for a spatial modulator; a plurality of pointers to bit position array on said backplane; and pointer controller means for controlling said plurality of pointers and manipulating pointers in sequence. Combination teaches applicant's cliamed novel and invention and the do obviate

Claims 126-130 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Schefer et al., in view of Dingwell, Chiu et al., Hustan et al. ands Pittitt et al.

Schefer et al., display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements; also teaches circular and non-circular buffer (shift register). Dingwall teaches storing a first group of bit positions of a plurality of pixels in bit position arrays on a backplane, said first group of bit positions comprising a contiguous group of bit positions; storing second group of bit positions on backplane, second group of bit positions corresponding to a subset of said plurality of pixels; and combining on backplane first group and second group to thereby control a pulse width of one or more light modulating elements. Chiu et al. teaches group of bit positions is stored for a period of time on backplane to control pulse width control based on their weight. Hustan et al. teaches group of bit positions is stored for a shorter period of time on a backplane than another group of bit positions is stored on backplane and Pittitt et al. teaches summary bit to thereby control a pulse width of one more light modulating elements, summary bit is stored for a shorter period of time on said backplane than group of bit positions is stored on backplane. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 131-141 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Schefer et al., in view of Hustan et al. and Coker et al.

Schefer et al., display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width

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starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements; also teaches circuilar and non-circular buffer (shift register). Hustan et al. teaches group of bit positions is stored for a shorter period of time on s backplane than another group of bit positions is stored on backplane and Coker et al. teaches an array of circuits shifting voltage level; a selectable logic function based on a memory bit; and means for controlling one or more light modulating elements, wherein a constant voltage source is used for said array of circuits, voltage level is outputted per weight of each bit, also teaches P-channel and N-channel transistor, pull-up and pull-down circuitry and logic function controls the binary sistae of each bit . Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 142-151 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Schefer et al., in view of Hustan et al. Chiu et al., Wood and Coker et al.

Schefer et al., display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby controlling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends, also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements; also teaches circuilar and non-circular buffer (shift register). Hustan et al. teaches group of bit positions is stored for a shorter period of time on s backplane than another group of bit positions is stored on backplane. Hustan et al. teaches; display system providing available memory on a spatial light modulator; and means for reallocating said available memory for data on said spatial light modulator, wherein space allocated is based on the length of time that said data needs to stay resident on said spatial light modulator and wherein said data is processed to control electrodes on said spatial light modulator and backplane further comprises a pointer memory array, said memory pointers are held in said pointer memory array and instruction memory, ROM and RAM and achieves gamma correction. Chiu et al. teaches group of bit positions is stored for a period of time on backplane to control pulse width control based on their weight and Master-slave bit operation and master , slave bits are accessed randomly. Wood teaches MRAM memory array and the ROM and MRAM provide program memory and workspace for the CPU, and special processing hardware may be provided to assist the CPU to perform the large number of arithmetic operations required to convert all but the simplest models into a two dimensional scene. and Coker et al. teaches an array of circuits shifting voltage level; a selectable logic function based on a memory bit; and means for controlling one or more light modulating elements, wherein a constant voltage source is used for said array of circuits, voltage level is outputted per weight of each bit, also teaches P-channel and N-channel transistor, pull-up and pull-down circuitry and logic function controls the binary state of each bit . Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 152-159 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Schefer et al., in view of Nelson and Holmes

Schefer et al., display driver driving electrode using a pulse width controlled by digital recursive feedback to thereby comntrolling a pixel of a spatial light modulating element according to pixel values based on a image signal to be displayed, logically combining current ouput bit with next output bit to drive pixel electrode and each individual pulse width performing two series of count, when pulse width starts and pulse width ends also teaches sequencially (serial processing) processing bit processing element located on the driver IC substrate which controls light modulating elements; also teaches circuilar and non-circular buffer (shift register). Nelson teaches mapping m bit input pixel value into a non binary weighted single pulse using time based remapping to thereby control a light modulating element of a spatial light modulator. Holmes teaches a display unit driving by controlling light modulating element, display interface controller with recursive feedback of a visual display that includes array of lght modulating elemens and mapping an input pixel value for each pixel of an array of pixels to a first output pixel value using a first time base to generate first pulse width; and mapping said input pixel valuc to a second output pixel valuc using a second time basc to gencrate a second pulsc width to thereby reduce the worse case phase difference in adjacent pixels of a spatial light modulator, adjacent pixels of array of pixels have respective input pixel values that differ by 1 LSB bit. Combination teaches applicant's cliamed novely and invention and they do obviate.

Claims 160-168 lacks novelty under PCT article 33(2), and lacks an inventive step under PCT article 33(3) as being obvious over the combination of Holmes in view of Nelson, Wood, Zhang, Gottfried et al. and Suzuoki et al.

Holmes teaches a display unit driving by controlling light modulating element, display interface controller with recursive feedback of visual display that includes array of lght modulating elemens and mapping an input pixel value for each pixel of an array of pixels to a first output pixel value using a first time base to generate first pulse width; and mapping said input pixel value to a second output pixel

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value using a second time base to generate a second pulse width to thereby reduce the worse case phase difference in adjacent pixels of a spatial light modulator, adjacent pixels of array of pixels have respective input pixel values that differ by 1 LS bit. Nelson teaches mapping m bit input pixel value into a non binary weighted single pulse using time based remapping to thereby control a light modulating element of a spatial light modulator. Wood teaches MRAM memory array and the ROM and MRAM provide program memory and workspace for the CPU, and special processing hardware may be provided to assist the CPU to perform the large number of arithmetic operations required to convert all but the simplest models into a two dimensional scene. Zhang, Gottfried et al. and Suzuoki et al. teaches a MRAM array of MRAM storage bits for a spatial light modulator, said MRAM storage bits being arranged in MRAM columns; and bit lines for each of said MRAM columns, wherein said bit lines support a first and a second driver on opposite sides of said array, wherein said MRAM storage bits are for a spatial light modulator and ERAM storage bits . Combination teaches applicant's cliamed novely and invention and they do obviate.